IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	MEEUSEN
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For	:	RECEIVER

APPEAL BRIEF

On Appeal from Group Art Unit 9418

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Michael Ure
(Name)

(Signature and Date)

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I. REAL PARTY IN INTEREST

The real party in interest is NXP B.V., the successor in interest to the present assignee of record of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-10 are pending, all of which stand finally rejected and form the subject matter of the present appeal.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to an audio receiver for receiving, for example, a frequency modulated stereo multiplex signal. The stereo signal may be double side band with suppressed carrier (DSB-SC) modulated on a 38kHz carrier, with a 19kHz pilot tone

in the multiplex signal being used to reconstruct the carrier's phase and frequency for demodulation. In a prior art receiver, a FIR halfband filter with perfect anti-symmetrical amplitude response around exactly 38kHz is used such that the upper and lower side band perfectly reconstruct the stereo signal when they fold together, even though most of the upper side band is suppressed. The 38kHz must be phase-locked to the 19kHz pilot tone. Such a solution is complex and exacting. In the present invention, on the other hand, in one embodiment thereof, the analog stereo multiplex signal is converted into a time discrete digital stereo multiplex signal and then the time discrete digital stereo multiplex signal is shifted over a frequency of 19 kHz to extract at least one of the time-discrete digital stereo sum and the time discrete digital stereo difference signal. In another embodiment, two successive frequency shifts are carried out, each frequency shift being of 19kHz, for example.

The following analysis of independent claim 1 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
1. Method for a receiver having a signal path incorporating		
a tuner,	Fig. 1, 4	Page 3, lines 5-21
a frequency demodulator circuit for supplying an analog stereo multiplex signal comprising a baseband stereo sum signal, a 19 kHz stereo pilot and a stereo difference signal, which is double sideband amplitude-modulated on a suppressed 38 kHz subcarrier,	Fig. 1, 5	Page 3, lines 5-21
a sampler for converting the analog stereo multiplex signal into a time discrete	Fig. 1, 6	Page 3, lines 5-21

digital stereo multiplex signal and		
a stereo decoder for decoding the time discrete digital stereo multiplex signal into a time-discrete digital stereo sum and a time discrete digital stereo difference signal,	Fig. 1, 7	Page 3, lines 5-21
wherein the analog stereo multiplex signal is converted into a time discrete digital stereo multiplex signal and then the time discrete digital stereo multiplex signal is shifted over a frequency of 19 kHz to extract at least one of the time-discrete digital stereo sum and the time discrete digital stereo difference signal.	Fig. 2	Page 3, line 22 to page 4, line 2; page 4, lines 12-15 and 29-32.

The following analysis of independent claim 5 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
5. Receiver having a signal path incorporating		
a tuner,	Fig. 1, 4	Page 3, lines 5-21
a frequency demodulator circuit for supplying an analog stereo multiplex signal comprising a baseband stereo sum signal, a 19 kHz stereo pilot and a stereo difference signal, which is double sideband amplitude-modulated on a suppressed 38 kHz subcarrier,	Fig. 1, 5	Page 3, lines 5-21
a sampler for converting the analog stereo multiplex signal into a time discrete digital stereo multiplex signal and	Fig. 1, 6	Page 3, lines 5-21
a stereo decoder for decoding the time discrete digital stereo multiplex signal into a time-discrete digital stereo sum and a time discrete digital stereo difference signal,	Fig. 1, 7	Page 3, lines 5-21
wherein the stereo decoder comprises two frequency shifting circuits connected in series with one another.	Fig. 2, 21 and 22	Page 4, lines 12-15 and 29-32.

The following analysis of independent claim 9 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
9. Stereo decoder		
in a receiver	Fig. 1, 1	Page 3, lines 5-21
with a frequency demodulator circuit,	Fig. 1, 10	Page 3, lines 5-21
wherein the stereo decoder comprises two frequency shifting circuits connected is series with one another.	Fig. 2, 21 and 22	Page 4, lines 12-15 and 29-32.

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. under 35 USC 102, claims 1 and 4 are anticipated by Therssen.

2. under 35 USC 102, claims 1-10 are anticipated by Wildhagen.

VII. ARGUMENT

I. Rejection of Claims 1 and 4 as Anticipated by Therssen

Therssen is described in the BACKGROUND section of the specification. In Therssen, a mixer M2 (Fig. 1) functions as a synchronous amplitude detector (page 6, lines 7-12). Based on the detected amplitude of the stereo multiplex signal output SMO, a decision is made to enable mono output or stereo output (MSS block). The block M2 does not shift the time discrete digital stereo multiplex signal over a frequency of 19 kHz to extract at least one of the time-discrete digital stereo sum and the time discrete digital stereo difference signal, as contended in the rejection.

That is, in the present invention, extraction of the sum or difference signal is accomplished by means of the frequency shift of 19kHz. In Therssen, extraction of the sum or difference signal (IC1 or IC2) is accomplished as illustrated in Fig. 2 thereof by the circuits QMF (time-discrete halfband lowpass filter) and IC (interpolation circuit). This extraction occurs regardless of the operation of M2. The only effect of M2 is to influence whether a mono or stereo output is finally output.

Accordingly, it may be seen that Therssen fails to anticipate the invention of claim 1.

Claim 4 specifies that time discrete digital stereo multiplex signal is shifted over a frequency of 19 kHz to extract the time discrete digital stereo difference signal, and that the time discrete digital stereo sum signal is extracted from the time discrete digital stereo multiplex signal in a parallel branch by a second low pass filter. Therssen does not shift the time discrete digital stereo multiplex signal over a frequency of 19 kHz to extract the

time discrete digital stereo difference signal, as has already been seen. Therssen therefore fails to anticipate claim 4.

II. Rejection of Claims 1-10 as Anticipated by Wildhagen

With respect to Wildhagen, Figure 5 thereof, the rejection erroneously contends that "the time discrete digital stereo multiplex signal [m] is shifted over a frequency of 19kHz (37) to extract at least one of the time-discrete sum and the time discrete digital stereo difference signal (through 20, 21, 24), and further shifted (by 18) and having a lowpass filter (21 or 24)."

The block 37 is a digital phase lock loop, and the block 18 is an up-sampling circuit. As described at col. 4, lines 42-45, "The DPLL-circuit 37 [and 18] generates a carrier for the coherent amplitude demodulation of the stereo-difference signal $m_d(t)$ and a carrier for the coherent pilot carrier detection, i.e., the detection of a stereo transmitter."

It will be appreciated that the DPLL circuit does not perform any frequency shifting of the time discrete digital stereo multiplex signal m itself. What the DPLL circuit does is to derive a first time reference signal from the time discrete digital stereo multiplex signal and a second time reference signal from the first time reference signal.

Accordingly, it may be seen that Wildhagen does not anticipate claim 5.

With respect to claim 9, the DPLL circuit of Wildhagen cannot be considered to be "two *frequency shifting* circuits connected is series with one another." As made clear in the present specification, a frequency shifting circuit is used to shift the center frequency of an information-bearing signal (not a carrier signal or reference signal). Accordingly, it may be seen that Wildhagen does not anticipate claim 9.

With regard to dependent claims 6-8 and 10, these claims depend from independent claim 5, which has been shown to be patently distinguishable over the cited reference. Accordingly, these claims are also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claim.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: 5/13/2008

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IX. APPENDIX: THE CLAIMS ON APPEAL

1. Method for a receiver having a signal path incorporating a tuner, a frequency demodulator circuit for supplying an analog stereo multiplex signal comprising a baseband stereo sum signal, a 19 kHz stereo pilot and a stereo difference signal, which is double sideband amplitude-modulated on a suppressed 38 kHz subcarrier, a sampler for converting the analog stereo multiplex signal into a time discrete digital stereo multiplex signal and a stereo decoder for decoding the time discrete digital stereo multiplex signal into a time-discrete digital stereo sum and a time discrete digital stereo difference signal, wherein the analog stereo multiplex signal is converted into a time discrete digital stereo multiplex signal and then the time discrete digital stereo multiplex signal is shifted over a frequency of 19 kHz to extract at least one of the time-discrete digital stereo sum and the time discrete digital stereo difference signal.

2. Method as claimed in claim 1, wherein the 19 kHz shifted signal is further shifted with 19 kHz and then the stereo difference signal is extracted by a low pass filter.

3. Method as claimed in claim 2, wherein in front of the low pass filter a lower sideband of the stereo difference signal is extracted by a complex filter from the signal shifted twice.

4. Method as claimed in claim 1, wherein the time discrete digital stereo multiplex signal is shifted over a frequency of 19 kHz to extract the time discrete digital stereo difference

signal, and wherein the time discrete digital stereo sum signal is extracted from the time discrete digital stereo multiplex signal in a parallel branch by a second low pass filter.

5. Receiver having a signal path incorporating a tuner, a frequency demodulator circuit for supplying an analog stereo multiplex signal comprising a baseband stereo sum signal, a 19 kHz stereo pilot and a stereo difference signal, which is double sideband amplitude-modulated on a suppressed 38 kHz subcarrier, a sampler for converting the analog stereo multiplex signal into a time discrete digital stereo multiplex signal and a stereo decoder for decoding the time discrete digital stereo multiplex signal into a time-discrete digital stereo sum and a time discrete digital stereo difference signal, wherein the stereo decoder comprises two frequency shifting circuits connected in series with one another.

6. Receiver as claimed in claim 5, wherein the stereo decoder comprises a low pass filter extracting the stereo difference signal.

7. Receiver as claimed in claim 5, wherein the stereo decoder comprises a complex filter extracting a lower sideband of the stereo difference signal.

8. Receiver as claimed in claim 5, wherein the stereo decoder comprises a second low pass filter extracting the stereo sum signal in a parallel branch.

9. Stereo decoder in a receiver with a frequency demodulator circuit, wherein the stereo decoder comprises two frequency shifting circuits connected is series with one another.

10. Stereo decoder as claimed in claim 9, wherein the frequency shifting circuits are phase rotators.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE